Amendments to the Specification:

Please reverse the order of paragraphs [0001] and [0002] along with their headings such that the first two paragraphs read as follows:

CROSS REFERENCE TO RELATED APPLICATION

~~[0002]~~ [0001] This application claims the benefit under 35 U.S.C. §120 of, and is a continuation-in-part of, of U.S. Patent Application Serial No. 10/235,628, by Chan et al., entitled "Display Processor Integrated Circuit With On-Chip Programmable Logic For Implementing Custom Enhancement Functions," filed September 4, 2002 (the subject matter of the above-identified patent application is incorporated herein by reference).

TECHNICAL FIELD

~~[0001]~~ [0002] This application relates to deinterlacing of video information.

Please replace paragraph [0009] with the following replacement paragraph.

[0009] A display processor integrated circuit (for example, for a television or for a digital camera) includes a display processor portion and an on-chip programmable logic portion. The on-chip programmable logic portion can be configured or programmed to implement custom video and/or image enhancement functions. The display processor portion performs block-based motion detection. Rather than attempting to match a block of pixels in one field with a corresponding block of pixels in a subsequent field as is often done in motion compensation, the block-based motion detection performed by the display processor integrated circuit generates a sum value and a difference value from pixel pairs in corresponding pixel locations in the block in **the** field preceding the field of interest and the field subsequent to the field of interest. If these sum and difference values have a

predetermined relationship to one another, then the block is, in one particular embodiment, determined to exhibit the motion characteristic.

Please replace paragraph [0014] with the following replacement paragraph.

[0014] Figure 2 is a simplified block diagram of the integrated circuit ~~9~~ of the video display device of Figure 1.

Please replace paragraph [0037] with the following replacement paragraph.

[0037] Once the interpolation process is completed for all the blocks of the segment, then ~~segment buffer~~**FIFO** 30 contains all the newly interpolated pixels for the blocks in that segment. These blocks of newly interpolated pixels are stored by memory control block 23 in RAM 15. When the resulting field of "deinterlaced" video is to be output, then the segment of newly interpolated pixels is combined with the original segment and the resulting "deinterlaced" segment of blocks is output onto output bus 31 to FIFO 32. Each pixel is represented by 16 bits, and 8 pixels (all the pixels, both original and interpolated, in a column of the segment) are output onto bus 31 at the same time. Output bus 31 is therefore 128 bits wide. FIFO 32 contains 960 such 128-bit wide words.

Please replace paragraphs [0052]-[0053] with the following replacement paragraphs.

[0052] The successive sets of three gradients are examined to look for a first pattern. The first pattern involves at least four gradients in the top row of gradients being digital ones, but where the corresponding gradients below those in the next row down are all digital zeros, and the corresponding gradients below those in the next row down are all digital zeros. If such a first pattern of gradients is found, then more gradients are determined and examined to see if a second pattern exists to the right of the first pattern. The second pattern exists where number G of consecutive gradients in the top row of gradients are digital ones, where the G gradients below those in the next row down one all digital ones, and where the G gradients below those in the next row down are all digital zeros. Number G can be set to be, for example, minimum of two. If this second pattern is found, then more gradients are determined and examined to see if a third pattern exists to the right of the second pattern. This third pattern exists where number H consecutive gradients in the top row of gradients are all digital zeros, where the H gradients below those in the next row down ~~one~~<u>are</u> all digital ones, and where the H gradients below those in the next row down are all digital zeros. Number H can be set to be, for example, in the range of four to seventeen. If this pattern is found, then the number of consecutive ones in the second row of this pattern is stored. If this third pattern of gradients is found, then more gradients are determined and examined to see if a fourth pattern exists to the right of the third pattern. The fourth pattern exists where at least four consecutive gradients in the top row of gradients are digital zeros, where the corresponding gradients below those in the next row down one all digital zeros, but where the corresponding gradients below those in the next row down are all digital ones. If these four patterns are found in order from left to right in the set of gradients, and if all the digital ones have the same sign, then a determination is made that a "left tilt" exists. Left tilt luminance low angle spatial interpolation is performed by taking the number stored when the third pattern was detected, and dividing this number by two. If, for example, the number stored when the third pattern was detected was seven, then the

result of dividing by two yields the value of three (plus a remainder which is discarded). The pixel in the row above the pixel of interest but three pixels to the left is averaged with the pixel in the row below the pixel of interest but three pixels to the right. This average is the left tilt luminance low angle spatial interpolation result.

[0053] If left tilt luminance low angle spatial interpolation is not performed, then the same process is repeated to look for the conditions of right tilt luminance low angle spatial interpolation. The first pattern to be looked for at the left of the set of gradients exists where at least four consecutive gradients in the top row of gradients are digital zeros, where the corresponding gradients below those in the next row down are all digital zeros, but where the corresponding gradients below those in the next row down are all digital ones. The second pattern to be looked for to the right of the first pattern exists where the number G consecutive gradients in the top row of gradients are digital zeros, where G gradients below those in the next row down are all digital ones, and where G gradients below those in the next row down are all digital zeros. Number G can be from 4 to 17. If this pattern is found, the number of consecutive ones in the second row of this pattern is stored. The third pattern to be looked for to the right of the second pattern exists where H consecutive gradients in the top row of gradients are digital ones, where H gradients below those in the next row down are all digital ones, and where H gradients below those in the next row down are all digital zeros. Number H can be set to, for example, minimum of two. The fourth pattern to be looked for to the right of the third pattern exists where at least four consecutive gradients in the top row of gradients are digital ones, where the corresponding gradients below those in the next row down are all digital zeros, and where the corresponding gradients below those in the next row down are all digital zeros. If these four patterns are detected, and if all gradient digital one values have the same sign, then right tilt ~~low~~ luminance **low** angle spatial interpolation is performed. The number stored when the second pattern was detected is divided by two. If, for example, the number stored when the third pattern was detected was seven, then the result of dividing by two yields the value of three (plus a remainder which is discarded). The pixel in the row above the pixel of interest but three pixels to the right is

averaged with the pixel in the row below the pixel of interest but three pixels to the left. This average is the right tilt luminance low angle spatial interpolation result.

Please replace paragraph [0060] with the following replacement paragraph.

[0060] As set forth above in connection with Figure 8, a decision (step 102) is made for each block of a segment whether motion has been detected. Then, after this decision has been made for all the blocks of the segment, the first missing row of pixels is generated for each of the blocks of the segment. Then the next missing row of pixels is generated for each of the blocks of the segment. In this manner, rows of missing pixels are generated, row by row, from top to bottom. The high angle interpolation uses one pixel above the pixel to be generated and one pixel below the pixel to be generated. The low angle interpolation uses pixels in two rows above the pixel to be generated and pixels in two rows below the pixel to be generated. Accordingly, once the second row of missing interline gap pixels has been generated for the blocks of the current segment, the top row of original pixels of the segment is no longer required for the ~~generated~~generation of new pixels. This is true regardless of whether low angle spatial interpolation is used or not.

Please replace paragraph [0063] with the following replacement paragraph.

[0063] This manner of pipelined loading of segment buffers 27, 28 and 29 (the overwriting of just used but no longer needed pixel data with new lines of pixel data at the same time that other pixel data is being read out of the segment buffers and is being used to perform interpolation) reduces memory bandwidth requirements of the external memory bus and allows a lower operating frequency of the memory control block 23 and

the external memory block 15. This eases design ~~requirement~~requirements on memory control block 23 and reduces system cost by allowing the use of low cost, low performance external DRAMs. Segment buffers 27-29 are dual-port memories so that memory control block 23 can write original pixel data into the segment buffers at the same time that process block 26 reads pixel data out of the segment buffers.

Please replace paragraph [0072] with the following replacement paragraph.

[0072] In some embodiments, PGA block 10 interfaces to the memory control block 23 such that PGA block 10 accesses portions of the fields of pixels in RAM 15 that are not being used by the other blocks of Figure 2. Memory control block 23 may, for example, involve a microcoded DMA state machine that receives and executes DMA commands from a microcode control store. In ordinary operation, the DMA state machine executes DMA commands such that the DMA state machine carries out the loading of segment buffers 27~~17~~-29 as set forth in the description of interpolation above. PGA block 10 is, however, also able to write DMA commands into to a part of the microcode control store, thereby allowing PGA block 10 to cause a DMA transfer of an amount of pixel data from RAM 15 to PGA block 10. PGA block 10 can then manipulate the pixel data. PGA block 10 can cause the resulting pixel data to be written back into RAM 15 by writing an appropriate DMA command into the control store. The DMA state machine executes the DMA command, thereby retrieving the pixel data from PGA block 10 and places it back into RAM 15 at a location identified by the DMA command. Although a DMA technique is set forth here by which PGA block 10 can access pixel data in RAM 15, other techniques for giving PGA block 10 access to this pixel data can be employed. Accordingly, various modifications, adaptations, and combinations of various features of the described embodiments can be practiced without departing from the scope of the invention as set forth in the following claims.